ABSTRACT

In accordance with a preferred embodiment, a time-interleaved (or multi-phase) architecture is provided having individual control of a plurality of output signals or phases. The time-interleaved architecture may be implemented using a first set of delay cells such as those in a ring oscillator or a delay line device receiving overall control of its output signals by a global control signal. The global control signal may be issued by a phase-locked loop, delay-locked loop, or other like structure. A second set of delay cells is provided to further delay the output signals produced by the first set of delay cells. The second set of delay cells are controlled by individual control signals uniquely calibrated in accordance with a preferred embodiment of the invention to provide uniform (or substantially) uniform time spacing between output signals.